Notice of Allowability	Application No.	Applicant(s)	
	10/695,857	TSUCHIDA, KENJI	
	Examiner	Art Unit	
	Tuan T. Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to _____.

2. ☒ The allowed claim(s) is/are *1-20*.

3. ☒ The drawings filed on *30 October 2003* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____.
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 10/30/03
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☒ Other *Attachment A: Search History*.

VAN THU NGUYEN
PRIMARY EXAMINER

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 10/30/03 was filed after the mailing date of the present application. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Allowable Subject Matter

3. Claims 1-20 are allowed.

4. The following is an examiner's statement of reasons for allowance:

The prior art of record fail to disclose, in combination with other cited limitations, a semiconductor integrated circuit device comprising a memory cell array in which memory cells each of which stores information by using a magneto-resistive effect are arranged a matrix; a constant current circuit which is connected first potential supply source and used to write data each memory cell in the memory cell array; and a current peak suppressing circuit configured to suppress a current peak that generated at a write start timing due to charges which flow out from a parasitic capacitance connected to an output terminal the constant current circuit or charges which flow into the parasitic capacitance, the current peak suppressing circuit having switch circuits to selectively supply an output from the constant current circuit to a specific write line, and a circuit portion which connects one of two terminals of each of the switch circuits to a

second potential supply source having a potential different from that of the first potential supply source before the timing of the start of the write operation and short-circuits the two terminals of each of the switch circuits immediately after the start of the write operation as recited in claims 1-17.

The prior art of record further fail to disclose a semiconductor integrated circuit device comprising a plurality of memory cell blocks which memory cells each of which stores information by using a magneto-resistive effect are arranged in a matrix; a constant current circuit which is used to write data in each memory cell in the memory cell blocks, the constant current circuit being shared by two adjacent memory cell blocks; switch circuits which are arranged in correspondence with each memory cell block and configured to selectively connect an output from the constant current circuit to a specific write line; and a current peak suppressing circuit configured to suppress a current peak at a timing of a start a write operation as recited in claim 18.

The prior art of record further fail to disclose a semiconductor integrated circuit device comprising a plurality of memory cell blocks in which memory cells each of which stores information by using a magneto-resistive effect are arranged matrix; a constant current circuit which used to write data in each memory cell in the memory cell blocks; switch circuits which are arranged in correspondence with each memory cell block and configured to selectively connect an output from the constant current circuit to a specific write line; and a current peak suppressing circuit configured suppress a current peak at a timing of a start of a write operation, wherein the constant current circuit and the current peak suppressing circuit are shared by two adjacent memory cell blocks as recited in claim 19.

The prior art of record also fail to disclose a semiconductor integrated circuit device comprising write lines to write information in memory cells each of which stores information by using a magneto-resistive effect; a constant current circuit which is connected to a first potential supply source and used to write data the memory cells; switch circuits each having one terminal connected one of the write lines and the other a corresponding terminal connected to an output terminal of the constant current circuit in parallel; and a current peak suppressing circuit which has a circuit portion to which said one terminal of each of the switch circuits connected and is configured to connect one of the two terminals of each of the switch circuits to a second potential supply source having a potential different from that of the first potential supply source before a timing of a start of a write operation and short-circuit the two terminals of each of the switch circuits immediately after the start of the write operation as recited in claim 20.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Nguyen whose telephone number is (571) 272-1880. The examiner can normally be reached on Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

January 10, 2005

Tuan T. Nguyen
Patent Examiner
Art Unit 2824

VAN THU NGUYEN
PRIMARY EXAMINER